(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 191 603 A2

(12) EUROPEAN PATENT APPLICATION

(43) Date of publication:
27.03.2002 Bulletin 2002/13

(51) Int Cl.[7]: **H01L 29/78**

(21) Application number: **01122746.9**

(22) Date of filing: **21.09.2001**

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **22.09.2000 US 668663**

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(54) Trench MOS device and termination structure

(57) A termination structure for power trench MOS devices is disclosed. The MOS devices can be Schottky diode, IGBT or DMOS depending on what kinds of the semiconductor substrate are prepared. The termination structure comprises: a semiconductor substrate having a trench formed therein; a MOS gate as a spacer formed on a sidewall of the trench; a termination structure oxide layer formed in the trench to cover a portion of the spacer and to cover a bottom of the trench; and a first electrode and a second electrode are, respectively, formed on a bottom surface and upper surface of the semiconductor substrate. The trench is formed from a boundary of the active region to an end of the semiconductor substrate. The trench MOS devices are formed in the active region. In addition for IGBT and DMOS, the second electrode is isolated from MOS gate by an oxide layer; however, for Schottky diode, the second electrode is directed contact to the MOS gate.

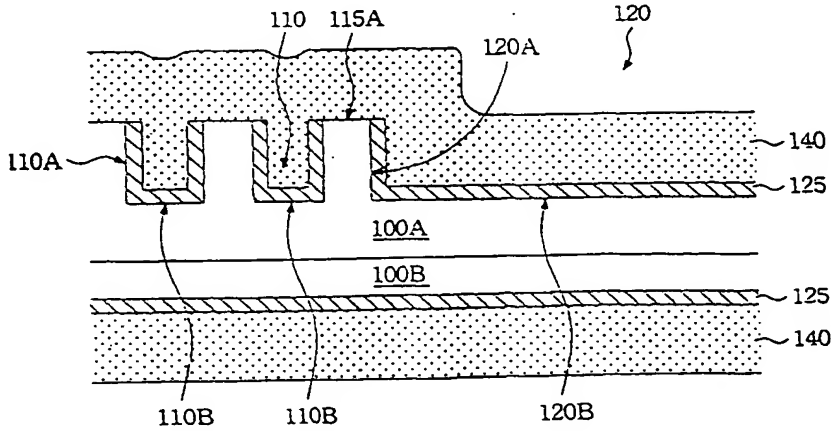

FIG.3

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Description

Field of the Invention

[0001] The present invention is related to a semiconductor device, specifically, to a novel termination structure for trench MOS devices so as to prevent leakage current.

Background of the Invention

[0002] Doubled diffused metal-oxide-semiconductor field effect transistor (DMOSFET), insulated gate bipolar transistor (IGBT), and Schottky diode are important power devices and use extensively as output rectifiers in switching-mode power supplies and in other high-speed power switching applications. For example, the applications include motor drives, switching of communication device, industry automation and electronic automation. The power devices are usually required carrying large forward current, high reverse-biased blocking voltage, such as above 30 volt, and minimizing the reverse-biased leakage current. There are several reports that trench DMOS, trench IGBT and trench Schottky diode are superior to those of with planar structure.

[0003] For power transistors are concerned, apart from the device in the active region for carrying large current, there is still required a termination structure design in the periphery of the active region usually at an end of a die so as to prevent voltage breakdown phenomena from premature. Conventional termination structures include local oxidation of silicon (LOCOS), field plate, guard ring, or the combination thereof. The LOCOS is generally known to have bird beak characteristic. In the bird beak, electric field crowding phenomena is readily to occur, which is due to high impact ionization rate. As a result, leakage current is increased and electrical properties of the active region are deteriorated.

[0004] For example, please refer to FIG.1, a semiconductor substrate with trench MOS structure for Schottky diodes, and a trench termination structure formed therein. The substrate is a heavily doped n+ substrate 10 and an epitaxial layer 20 formed thereon. A plurality of trench MOS 15 formed in the epitaxial layer 20. The trench MOS devices including epitaxial layer 20/gate oxide layer 25/ polysilicon layer 30 are formed in the active region 5. The boundary of the active region 5 to the edge of the die is a LOCOS region of about 6000Å in thick formed by conventional method.

[0005] For the purpose of lessening the electric field crowding issue, a p+-doping region 50 beneath LOCOS region is formed through ion implantation. The p+-doping region 50 is as a guard ring for reverse-biased blocking voltage enhancement. The anode (a metal layer) 55 is formed on the active region 5 and extends over p+ doping region 50 of LOCOS region. The object is to make the bending region of the depletion boundary far away from the active region 5. Although guard ring 50 can alleviate the electrical field crowding and relax the bending magnitude occurred near the active region, the adjacent region between p+ region 50 and beneath the bottom of the trench MOS device, as arrow indicated denoted by 60, is not a smooth curve. It will increase the leakage current and decrease the reverse-biased blocking capability. A similar situation occurred for field plate combines with guard ring. Furthermore, aforementioned prior art demanded more photo masks (at least four) to fabricate, and the processes are rather complicated. Still high cost for forming such structure is another inferior.

[0006] As forgoing several conventional termination structures can not solve the problems thoroughly. An object of the present invention thus proposes a novel termination structure. The new termination structure made the bending region of the depletion region far away from the active region, and depletion boundary is flatter than forgoing prior art. The manufacturing method provided by the present invention is even simpler than those prior arts. Since the termination structure and trench are formed simultaneously, it requires only three photo masks, low complicated processes and low cost.

Summary of the Invention

[0007] The present invention discloses a novel termination structure, which can be formed with trench MOS devices simultaneously. The MOS devices can be Schottky diode, DMOS or IGBT depending on what kinds of the semiconductor substrate are prepared. The termination structure and trench MOS devices comprising: a semiconductor substrate having a plurality of first trenches spaced each other and formed in an active region and having a second trench formed from a boundary of the active region to an end of the semiconductor substrate; a first-type MOS gate formed in each of the first trenches, and a second MOS gate as a spacer formed on a sidewall of the second trench; a termination structure oxide layer formed in the second trench to cover a portion of the spacer and to cover a bottom of the second trench; and a first electrode and a second electrode are, respectively, formed on a bottom surface and upper surface of the semiconductor substrate. The second electrode is located to cover the region from the active region through the spacer to a portion of the termination structure oxide layer so that a bending portion of the depletion region are distant from the active region.

Brief Description of the Drawings

[0008] The foregoing aspects and many of the attendant advantages of this invention will become more readily appreciated as the same becomes better understood by reference to the following detailed description, when taken in conjunction with the accompanying drawings, wherein:

FIG. 1 is a conventional trench Schottky diode devices and LOCOS plus guard ring as a termination structure.

FIG. 2 is a cross-sectional view of forming first trenches and second trench in a semiconductor substrate in accordance with the present invention.

FIG. 3 is a cross-sectional view of refilling the first trenches and the second trench with a first conductive material in accordance with the present invention.

FIG. 4 is a cross-sectional view of defining termination structure oxide layer to expose active region and spacer in accordance with the present invention.

FIG. 5A is a cross-sectional view of forming anode electrode and cathode electrode on both side of the semiconductor substrate so that Schottky diode and the termination structure are finished in accordance with the present invention.

FIG. 5B shows simulation results of equipotential lines and lines of electric force by using Schottky diode and the termination structure of the present invention.

FIG. 5C shows simulation results of leakage current of trench Schottky diode with and without the termination structure of the present invention.

FIG. 6 is a cross-sectional view of semiconductor substrate prepared for DMOS device and termination structure in accordance with the present invention.

FIG. 7 is a cross-sectional view of etching back first conductive layer and then performing a high temperature thermal oxidation process to form interconductive oxide layer in accordance with the present invention.

FIG. 8 is a cross-sectional view of defining termination structure oxide layer to expose active region and spacer in accordance with the present invention.

FIG. 9 is a cross-sectional view of forming source electrode and drain electrode on both side of the semiconductor substrate so that DMOS device and the termination structure are finished in accordance with the present invention.

FIG. 10 is a cross-sectional view of semiconductor substrate prepared for IGBT and termination structure in accordance with the present invention.

FIG. 11 is a cross-sectional view of defining termination structure oxide layer to expose active region and spacer in accordance with the present invention.

FIG. 12 is a cross-sectional view of forming emitter electrode and collector electrode on both side of the semiconductor substrate so that IGBT and the termination structure are finished in accordance with the present invention.

Detailed Description of the Preferred Embodiment

[0009] As depicted in the forgoing background of the invention, the conventional termination structure including local oxidation, electric field plate, guard ring, or the combination thereof, all of them do not solve completely the electric field crowding issues. The field crowding may still occur at different positions, depending on the design difference. The present invention proposes a novel trench termination structure and a method to make them. The novel trench termination structure is to overcome problems of electric field crowding issues. The newly trench termination provides a flat depletion boundary, and the bending region thereof is far away from the active region while encountered a reverse-bias voltage. Consequently, the novel termination structure can prevent breakdown phenomena from being occurred prematurely.

[0010] Moreover, the newly termination structure can be applied to any power transistors such as Schottky rectifier, DMOS, IGBT etc.. The most important fact is the trench MOS devices can be formed with the trench termination structure simultaneously.

[0011] Several exemplified embodiments will be successively illustrated.

[0012] The first preferred embodiment is to illustrate the method of forming trench termination structure and the Schottky diode simultaneously.

[0013] Please refer to FIG.2, a cross-sectional view shows a semiconductor substrate 100 comprised a first layer 100A having a first kind of conductive impurity doped (for example type n) and a base substrate 100B having a first kind of conductive impurity heavily doped (for example n+). First layer 100A is formed epitaxially on the base substrate 100B for forming Schottky contact and the base substrate is for forming ohmic contact while metal layers are formed thereon.

[0014] An oxide layer 101 is then formed on the first substrate 100A by CVD to about 2000 Å- 10000 Å. Next, a photoresist (not shown) is coated on the oxide layer 101 to define a plurality of first trenches 110 and a second trench 120. Each of the first trenches 110 is about 0.2-2.0 μm in width from cross-sectional view formed in the active region. The second trench 120 is spaced by a mesa 115 to the first trench 110 and formed from the boundary of the active region to an end of a semiconductor substrate 100 (or a die). The second trench 120 is to make depletion boundary flat and prevent electric field crowding.

[0015] Referring to FIG.3, after oxide layer 101 removal, a high temperature oxidation process to form gate oxide layer 125 is performed. The gate oxide layer 125 with a thickness between about 150 Å to 3000 Å is formed on the sidewalls 110A, 120A, bottoms 110B, 120B of the first and second trench 110, 120, and the mesa surface 115A. Alternatively, the gate oxide layer 125 can be formed by high temperature deposition to form HTO (high temperature oxide deposition) layer.

[0016] Subsequently, a first conductive layer 140 is formed by CVD on the gate oxide 125 and refilled the first trench 110 and the second trench 120, and at least with a height higher than the mesa115. The first conductive layer 140 is also formed on the backside of the semiconductor substrate 100E due to the CVD process. The first conductive layer is material selected from the group consisting of metal, polysilicon and amorphous silicon. Preferably, the first conductive layer 140 is about 0.5 to 3.0 μm. For preventing inner portion of first trench from forming voids therein, the polysilicon layer formed by LPCVD (low pressure CVD) which has good step coverage is preferred as the material of the first layer 140. However if the aspect ratio of first trench 110 over 5, amorphous silicon by PECVD would be preferred. The amorphous silicon has better gap filled characteristic than polysilicon. Surely, to make it with conductive properties, an amorphous silicon recrystallized process is needed.

[0017] Please refer to FIG. 4, an anisotropic etching is done to remove the excess first conductive layer 140 above the mesa surface 115A using the gate oxide layer 125 on the mesa 115 as an etching stop layer. After this process, a spacer 122 having a width (along cross-sectional view) about the same as the height of the second trench is formed on the sidewall 125A of the second trench 120.

[0018] Thereafter, a dielectric layer 150 for termination structure is formed. The dielectric layer is a TEOS layer either LPTEOS or PETEOS or O_3- TEOS or HTO layer. The dielectric layer 150 is between about 0.2-1.0 μm.

[0019] Next, a photoresist pattern 155 is coated on the dielectric layer 150 so as to define ranges of Schottky contacts. And then a dry etching using photoresist pattern 155 as a mask is carried out to expose mesa surface 115A and first conductive layer 140 of the first trench 110.

[0020] Turning to FIG. 5 after stripping the photoresist pattern 155, a backside unwanted layer removal is implemented to expose surface of the base substrate 100B. The unwanted layers are those layers formed on the backside of semiconductor substrate due to thermal oxidation process or CVD process for fabricating devices in the active region, including dielectric layer 150, first conductive layer 140, and gate oxide layer 125.

[0021] Thereafter, a sputtering process is performed to deposit second conductive layer so as to form Schottky contact regions 115 between second conductive layer and the first substrate 100A and to form cathode 160, which is an ohmic contact between second conductive layer and the second substrate 100B. Finally, a photoresist pattern 165 is formed on the second conductive layer to define anode electrode 160A. In a preferred embodiment, the anode 160A is formed from active region extending to the second trench 120 and at least to a region away from the active region by 2.0 μm. So the bending region of the depletion region is able to be far away from the active region.

[0022] FIG. 5B shows one of the electric properties of the trench MOS termination structure (shown in FIG. 5A). To simulate the reverse bias, for example, Schottky diode is exerted by a reverse bias. Hence, the cathode 160 has, for example, 100 Volt and anode 183 has 0 Volt. The numeral 180 denotes equipotential lines. In the figure, the voltages burdened by the equipotential lines from bottom to up are gradually decreased. The lines perpendicular to the equipotential lines 180 represent lines of electrical force. As shown in the figure, leakage current only generates in the active region and almost none in the depletion region under termination region. Moreover, the boundary of depletion region, denoted by label 180A, gives flat characteristic, and thus the voltage breakdown premature would not occur. It gives only a little bit of leakage current.

[0023] FIG.5C shows a comparison for reversed current curves of the trench MOS structure without termination structure 195 and with the termination structure 190 in accordance with the present invention. The termination structure merely increases reversed current by 8.8%. By contrast to 12.8% occurs in the conventional termination structure, the LOCOS combines with guard ring structure. The present invention gives significant improvement. In addition, it requires at least 4 photo masks by conventional manufacture processes compared to three masks only in the present invention (e.g., forming trench (1st), contact definition (2nd), and the second conductive layer etching to form anode (3rd)). The present invention gives a simpler process.

[0024] The second preferred embodiment using the termination structure according to the present invention is to form trench DMOS structure and termination structure.

[0025] Referring to FIG.6, for DMOS structure, the semiconductor substrate prepared is different from the case of forming Schottky diode but processes are quite similar. To forming DMOS and termination structure simultaneously, firstly, a semiconductor substrate 200 from the top to the bottom comprises a first layer 200A, a second layer 200B and a base substrate 200C. The first layer 200A and the second layer are formed on the base substrate 200C by epitaxial processes.

[0026] The first layer 200A having a p-type conductive doped impurities as a base layer and then a doping layer 203 with p-type conductive heavily doped impurities on the top portion of the first layer 200A. The second layer 200B is with n-type conductive doped impurities, and the third layer 200C with n-type conductive heavily doped impurities. Furthermore, a plurality of n+ regions are formed in the upper portion of the first layer 200A to cut p+ layer 203 to be as many n+ regions 204 and p+ region 204 by ion implantation, as is shown in FIG.6. The thickness of the first and second layer 200A and 200B are 0.5 μm - 5.0 μm and 3 μm - 30 μm, respectively.

[0027] Thereafter, please refer to FIG. 7, as forging method described in the first preferred embodiment, a

plurality of the first trenches 210 and the second trench 220 having a mesa 215 in between are formed firstly. The first trenches 210 are formed in the active region, through n+ regions 204. and the second trench 220 is formed in the region from the boundary of the active region to an end of the semiconductor substrate 200 (or a die).

[0028] Next, a high temperature oxidation process is performed to form a gate oxide layer 225 with a thickness of between about 150Å to 3000Å. Then, a conductive layer 240 selected from first polysilicon or amorphous silicon is refilled to the first trenches 210 and the second trench 220 and over mesa 215. An etching back step is then carried out to remove excess conductive layer 240 using gate oxide layer 225 on the surface of mesa 215A as a stopping layer. The gate oxide layer 225 removal above mesa is then followed using the n+ region 204 and the p+ region 203 as a stopping layer.

[0029] Subsequently, another thermal oxidation process is performed to form an inter-conductive oxide layer 245 by oxidizing a portion of the first conductive layer 240. Since the grain boundaries of the polysilicon can provide oxygen fast diffusion paths, the oxide layer formed by the polysilicon or amorphous silicon in the first trenches 210 and the second trench 220 are much thicker than that on the semiconductor substrate, the mesa surface 215A.

[0030] Referring to FIG.8 an etching back step is performed to remove thermal oxide layer 245 above surface of the first layer 200A, the n+ region 204 and p+ region 203. Worth to note, there is still a thermal oxide layer 245 on the spacer 240 of the second trench 220 and on the cop surface of first conductive layer 240 after this step to provide isolation function. A TEOS oxide layer 250 is then formed on all areas. A photoresist pattern is then formed on TEOS oxide layer 250 of the first layer 200A to define source contact regions.

[0031] Referring to FIG.9, before performing a sputtering process, the unwanted layers formed on the backside of semiconductor substrate (or say base substrate 200C) are removed firstly. The unwanted layers includes TEOS oxide layer 250, inter-conductive oxide layer 245, first conductive layer 240 and gate oxide layer 225 on the surface of base substrate 200C, which are formed simultaneously while making the devices in the active region.

[0032] Subsequently, a metal layer 260 deposition by sputtering is performed to form source contact on the first layer 200A and drain contact on the base substrate 200C i.e. the backside of the semiconductor substrate. As before, the metal layer 260 formed on the active region is still required to extend to the termination structure 220 by a distance at least about 2.0 μm so as to distant from the active region. To do this, a lithographic and an etching process are successively carried out as before.

[0033] The third preferred embodiment using the termination structure according to the present invention is to form trench IGBT structure and termination structure simultaneously.

[0034] Referring to FIG.10, for the trench MOS to be as the IGBT structure, the semiconductor substrate prepared is different from the case of forming Schottky diode but very similar to the semiconductor substrate using for trench DMOS device. In addition, the process is almost the same as the processes of fabricating trench DMOS. To forming IGBT and termination structure simultaneously, firstly, a semiconductor substrate 300 prepared from the top to the bottom comprises a first layer 300A, a second layer 300B, a third layer 300C and a base substrate 300D. The first layer 300A, the second layer 300B, and third layers 300C, are formed on the base substrate 300D by epitaxial processes.

[0035] The first layer 300A, 300B and 300C having doping type, and doping concentration similar to the semiconductor substrate shown in FIG.6. For example, first layer 300A is p-type base layer having upper portion n+ regions 304 and p^+ regions 303 in the upper portion of the p-base layer 302. The second layer 300B is a n-doping layer as a drift region and third layer 300C is a n+ layer 300B as a buffer layer. The base substrate 300D is, however, a p-type conductive impurities heavily doped region. The thickness of the first and the second layer 300A and 300B are 0.5 μm - 10.0 μm and 3 μm - 100 μm, respectively.

[0036] Turning to FIG.11, a plurality of the first trenches 310 are formed through the n+-doped region 304. The bottom of the first trenches 310 comes down to below the layer of the p-type-doped layer 302. Furthermore, the second trench 320 and first trench individual, each is spaced by a mesa 315 having 0.2 to 4.0 μm. The second trench 320 is formed at the boundary of the active region and is extended to an edge of the semiconductor substrate.

[0037] After an thermal oxidation process to form a gate oxide layer with a thickness of between 150Å to 3000Å, a refilled process with the first conductive material 340 such as polysilicon or amorphous silicon layer is deposited on the first trenches 310 and the second trench 320. An etch back process is then performed using gate oxide layer 325 on the surface of the mesa 315 as a stopping layer so that only the first trenches 310 and spacer in the second trench have the first conductive material 340.

[0038] As the second embodiment depicted before, gate oxide layer 325 on the surface of the first layer is then removed and then another thermal oxidation process is carried out to form inter-conductive oxide layer 345 for the conductive layer 340 and the metal layer (formed later) isolation. Thereafter, the thermal oxide 345 above mesa surface 315A is removed but a portion of the thermal oxide layer, which is on the first conductive layer in the first trenches 310 and the second trench 320 are remaining as an inter-conductive oxide layer.

[0039] Still referring to FIG. 11, a TEOS dielectric layer 350 deposition on all areas and photoresist pattern coating are followed successively as before. Thereafter,

an etching process is implemented to expose the n+-doped region 204 arid the p+-doped region.

[0040] FIG.12 shows backside unwanted layers on base substrate are removed before metal sputtering. After the second conductive layer, generally, a metal layer is formed on a surface of base substrate 300D to form collector electrode. After successively lithographic and etching process, the emitter electrode is formed on the surface of 300A, which contacts the p+ region 303 and n+ region 304. One end of emitter electrode is located at a distance away from active region.

[0041] The benefits of this invention are:

(1) The depletion boundary is flat and the bending region of depletion boundary is far away from active region. Both the properties are able to prevent voltage breakdown phenomena from occurring prematurely.
(2) The leakage current generated by the invention termination structure during reversed-biased is small than that of conventional LOCOS plus guard ring termination structures (8.8% vs. 12.8%).
(3) The method for fabricating the trench MOS device with termination structure is simpler than that of conventional methods. The invention termination structure requires less photo masks.

[0042] As is understood by a person skilled in the art, the foregoing preferred embodiment of the present o invention is an illustration of the present invention rather than limiting thereon. It is intended to cover various modifications and similar arrangements included within the spirit and scope of the appended claims, the scope of which should be accorded the broadest interpretation so as to encompass all such modifications and similar structure.

Claims

1. A termination structure for trench MOS devices, said termination structure comprising:

   a semiconductor substrate having a trench formed therein, said trench from a boundary of active region to an end of said semiconductor substrate, said trench MOS formed in said active region of said semiconductor substrate;
   a MOS gate as a spacer formed on a sidewall of said trench;
   a termination structure oxide layer formed in said trench to cover a portion of said spacer and to cover a bottom of said trench; and
   a first conductive layer, as a first electrode, formed on a bottom surface of said semiconductor substrate and a second conductive layer, as a second electrode, formed on an upper surface of said semiconductor substrate, where said upper surface of said semiconductor substrate is from said active region through said spacer to a portion of said termination structure oxide layer.

2. The termination structure of Claim 1, wherein said trench having a depth of between about 0.4-10 μm.

3. The termination structure of Claims 1-2, wherein said MOS gate comprises a conductive layer formed on a gate oxide layer.

4. The termination structure of Claims 1-2, wherein said trench MOS devices comprises power transistors.

5. The termination structure of Claims 1-4, wherein said power transistors is selected from the group consisting of Schottky diodes, DMOSs, and IGBTs, depending on what said semiconductor substrate are provided and whether said MOS gate having an inter-conductive oxide layer to isolate said conductive layer of said MOS gate from said second electrode.

6. A termination structure for trench MOS device, said termination structure and said trench MOS device comprising:

   a semiconductor substrate having a first trench and a second trench formed therein;
   a first MOS gate formed in said first trench, and a second MOS gate as a spacer formed on a sidewall of said second trench;
   a termination structure oxide layer formed in said second trench to cover a portion of said spacer and to cover a bottom of said second trench; and
   a conductive layer formed on a bottom surface of said semiconductor substrate as a first electrode and on an upper surface of said semiconductor substrate so as to form a second electrode.

7. The termination structure and trench MOS device of Claim 6, wherein said semiconductor substrate comprises a first layer and a base substrate, said first layer having a first kind of conductive impurities lightly doped and said base substrate having a first kind of conductive impurities heavily doped, said semiconductor substrate is for Schottky diode.

8. The termination structure and trench MOS device of Claims 6-7, wherein said first trench and second trench are formed in said first layer and having a depth of between about 0.4-10 μm.

9. The termination structure and trench MOS device

of Claims 6-8, wherein said first MOS gate and second MOS gate comprises a gate oxide layer on a bottom and a sidewall of said first trench and said second trench and a first conductive layer formed thereon so as to fill in said first trench and said second trench.

10. The termination structure and trench MOS device of Claims 6-9, wherein said first trench is formed in an active region and said second trench is formed from a boundary of said active region to an end of said semiconductor substrate.

11. The termination structure and trench MOS device of Claims 6-10, wherein said first conductive layer is a material selected from the group consisting of metal, polysilicon and amorphous silicon.

12. The termination structure and trench MOS device of Claims 6-11, wherein said second electrode is formed to contact said active region, said spacer and cover a portion of said termination structure oxide layer so that a bending region of a depletion region is distant from said boundary of said active region by at least 2μm in distance.

13. The termination structure and trench MOS device of Claims 6-12, wherein said semiconductor from top to bottom layer comprising a first layer, a second layer, a third layer and a base substrate, said first layer having p-type conductive impurities heavily doped, said second layer having p-type conductive impurities lightly doped, said third layer having n-type conductive impurities lightly doped, said base substrate having n-type conductive impurities heavily doped, still a plurality of n-type conductive impurities heavily doped region formed in said first layer and in an upper portion of said second layer, said semiconductor substrate is for DMOS device.

14. The termination structure and trench MOS device of Claims 6-13, wherein said first MOS gate has an inter-conductive oxide layer on a top to isolate said first conductive layer from said first electrode.

15. The termination structure and trench MOS device of Claims 6-13, wherein said first layer plus said second layer, said third layer are, respectively, between about 0.5μm-5.0μm and 3.0μm-30.0μm.

16. The termination structure and trench MOS device of Claims 6-15, wherein said semiconductor from top to bottom layer comprising a first layer, a second layer, a third layer, a forth layer, and a base substrate, said first layer having p-type conductive impurities heavily doped, said second layer having p-type conductive impurities lightly doped, said third layer having n-type conductive impurities lightly doped, said forth layer having n-type conductive impurities heavily doped, said base substrate having p-type conductive impurities heavily doped, still a plurality of n-type conductive impurities heavily doped region formed in said first layer and in an upper portion of said second layer, said semiconductor substrate is for IGBT device, still further, first MOS gate has an inter-conductive oxide layer on a top to isolate said first conductive layer from said first electrode.

17. A termination structure for trench MOS devices, said termination structure and trench MOS devices comprising:

a semiconductor substrate having a plurality of first trenches spaced each other and formed in an active region and having a second trench formed from a boundary of said active region to an end of said semiconductor substrate;
a first-type MOS gate formed in each of said first trenches, and a second MOS gate as a spacer formed on a sidewall of said second trench;
a termination structure oxide layer formed in said second trench to cover a portion of said spacer and to cover a bottom of said second trench; and
a conductive layer formed on a bottom surface of said semiconductor substrate as a first electrode and formed on an upper surface as a second electrode, said second electrode formed on said active region and extendedly formed on said spacer and on a portion of said termination structure oxide layer so that a bending portion of said depletion region is distant from said boundary of said active region by at least 2μm.

18. The termination structure and trench MOS devices of Claim 17, wherein said semiconductor substrate comprises a first layer and a base substrate, said first layer having a first kind of conductive impurities lightly doped and said base substrate having a first kind of conductive impurities heavily doped, said semiconductor substrate is for Schottky diode.

19. The termination structure and trench MOS devices of Claims 17-18, wherein said first trenches and second trenches having a depth of between about 0.4-10 μm.

20. The termination structure and trench MOS devices of Claims 17-19, wherein said first-type MOS gate and second MOS gate comprises a gate oxide layer on a bottom and a sidewall of said first trenches and said second trench and a first conductive layer formed thereon so as to fill in said first trenches and said second trench.

21. The termination structure and trench MOS devices of Claims 17-20, wherein said first conductive layer is a material selected from the group consisting of metal, polysilicon and amorphous silicon.

22. The termination structure and trench MOS devices of Claims 17-21, wherein said second electrode is formed to contact said active region, said spacer and cover a portion of said termination structure oxide layer so that a bending region of a depletion region is away from said active region.

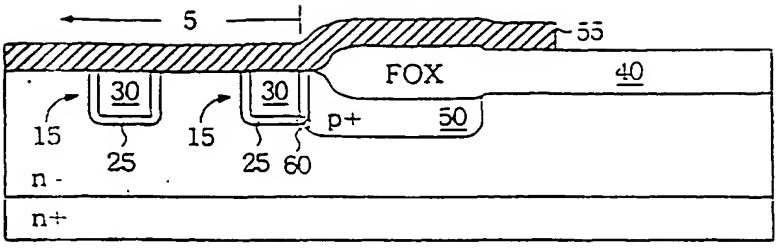

FIG.1

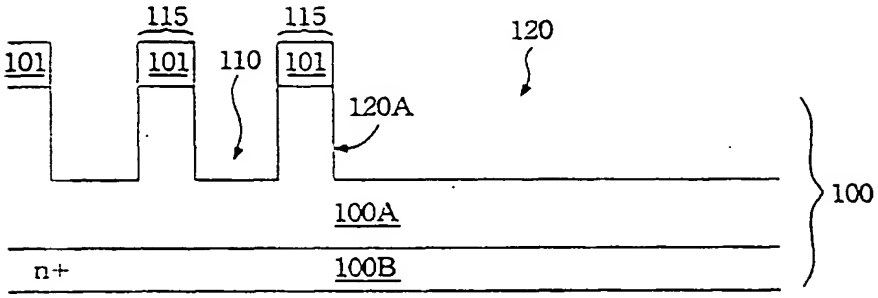

FIG.2

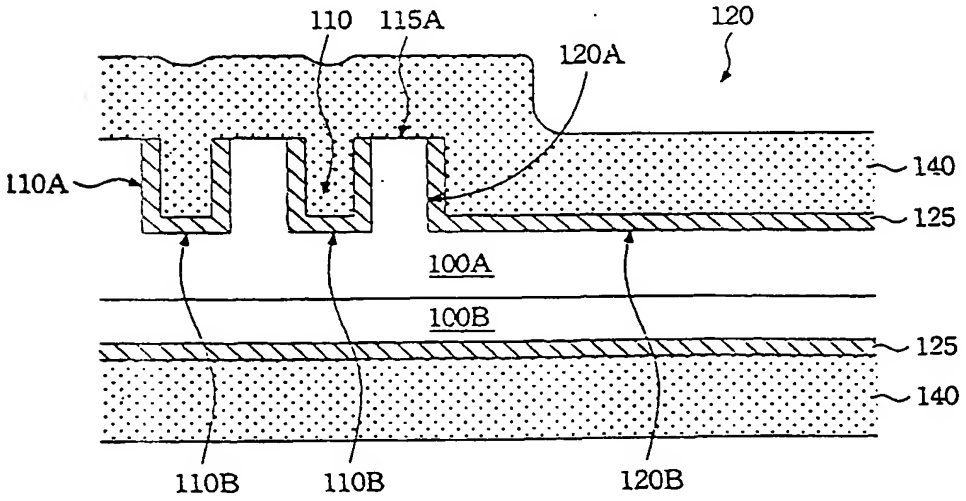

FIG.3

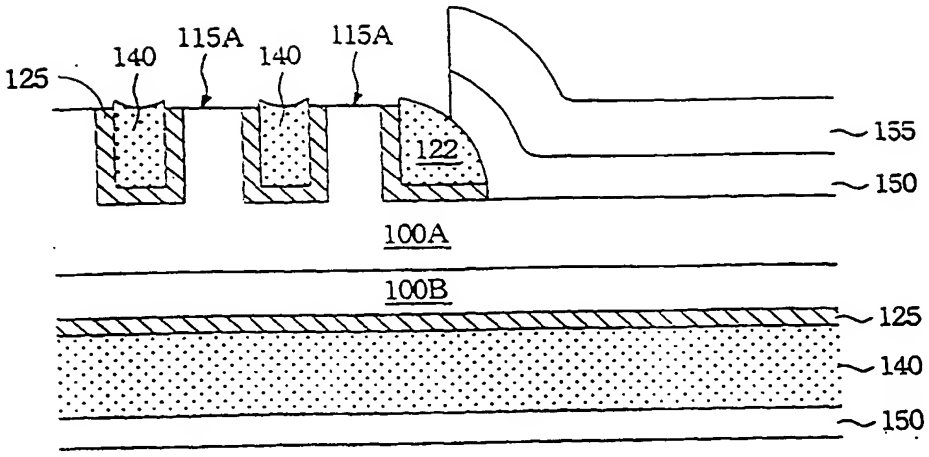

FIG.4

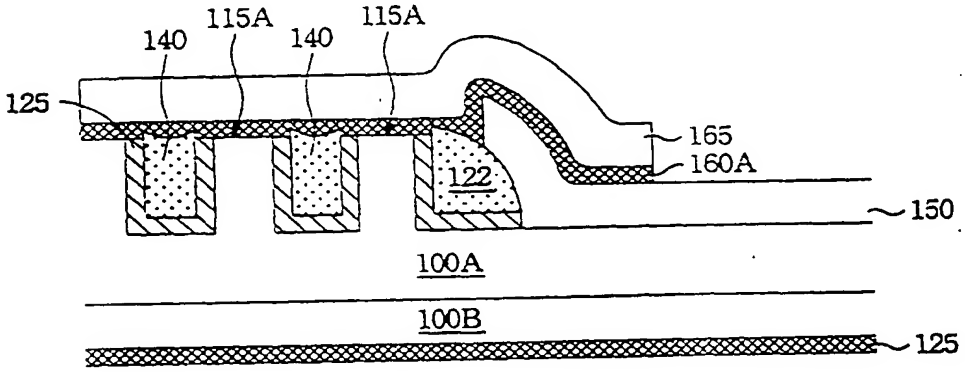

FIG.5A

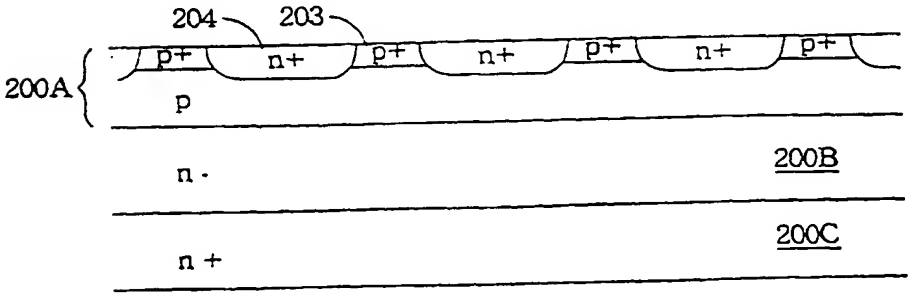

FIG.6

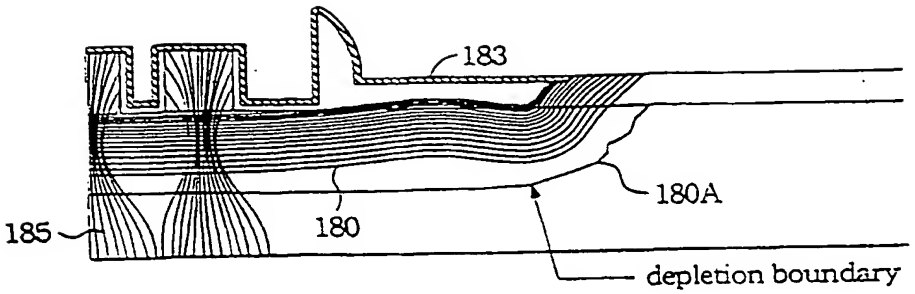
183
180A
185
180
depletion boundary

FIG.5B

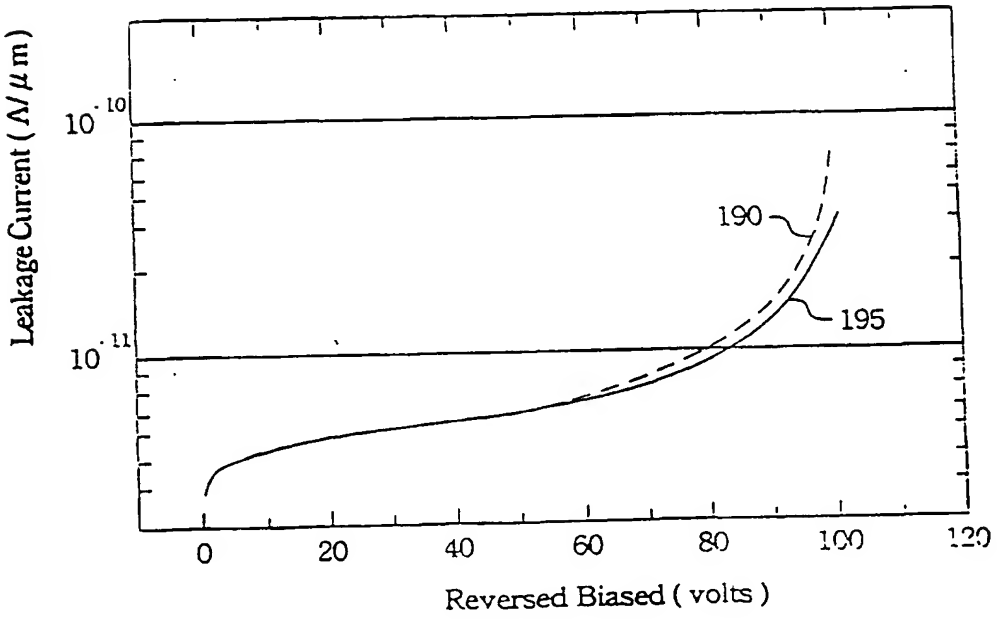
Leakage Current (A/ μ m)
10 -10
10 -11
190
195
0
20
40
60
80
100
120
Reversed Biased (volts)

FIG.5C

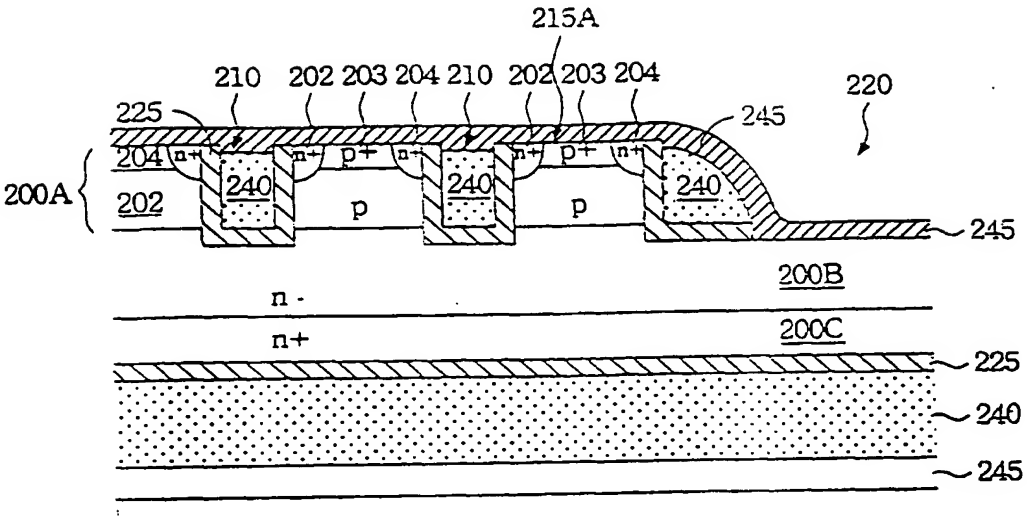
215A
210
202
203
204
210
202
203
204
220
225
245
200A
204
202
n+
p+
240
p
245
200B
n -
200C
n+
225
240
245

FIG.7

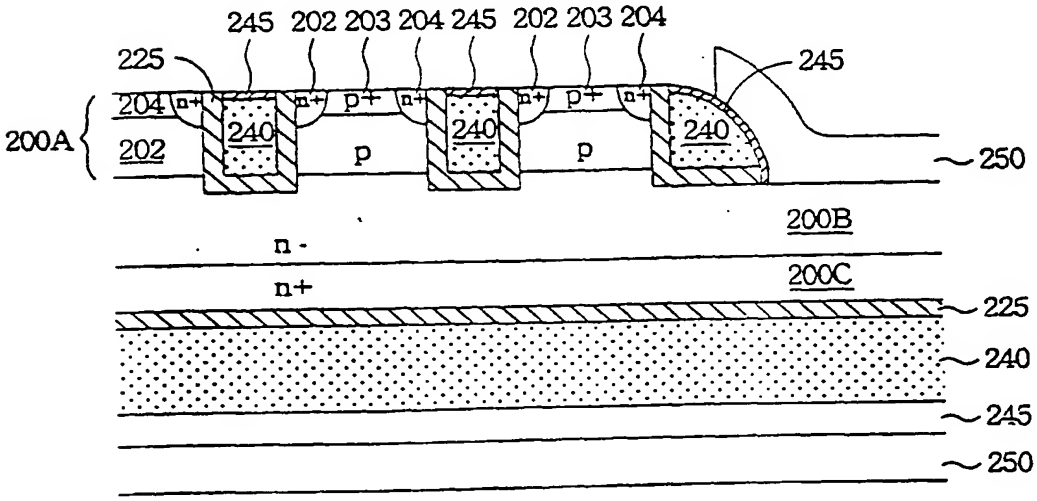
245
202
203
204
245
202
203
204
225
245
200A
204
202
n+
p+
240
p
250
200B
n -
200C
n+
225
240
245
250

FIG.8

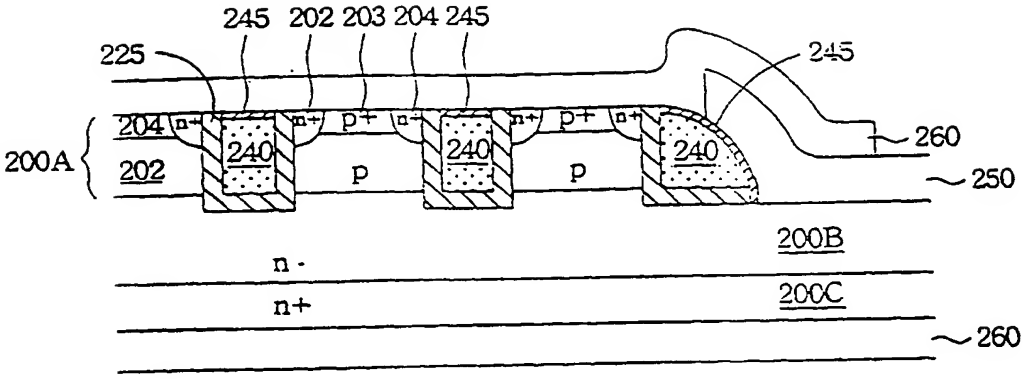
245 202 203 204 245
225
245
204
n+
240
n+
p+
n+
240
n+
p+
n+
240
260
200A
202
p
p
250
200B
n -
200C
n+
260

FIG.9

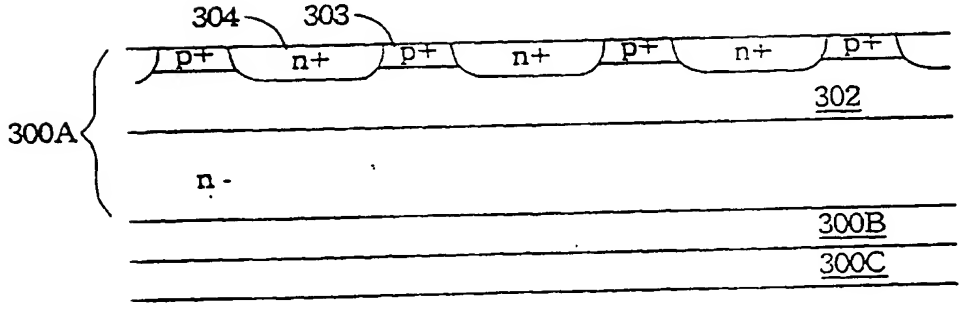
304
303
p+
n+
p+
n+
p+
n+
p+
302
300A
n -
300B
300C

FIG.10

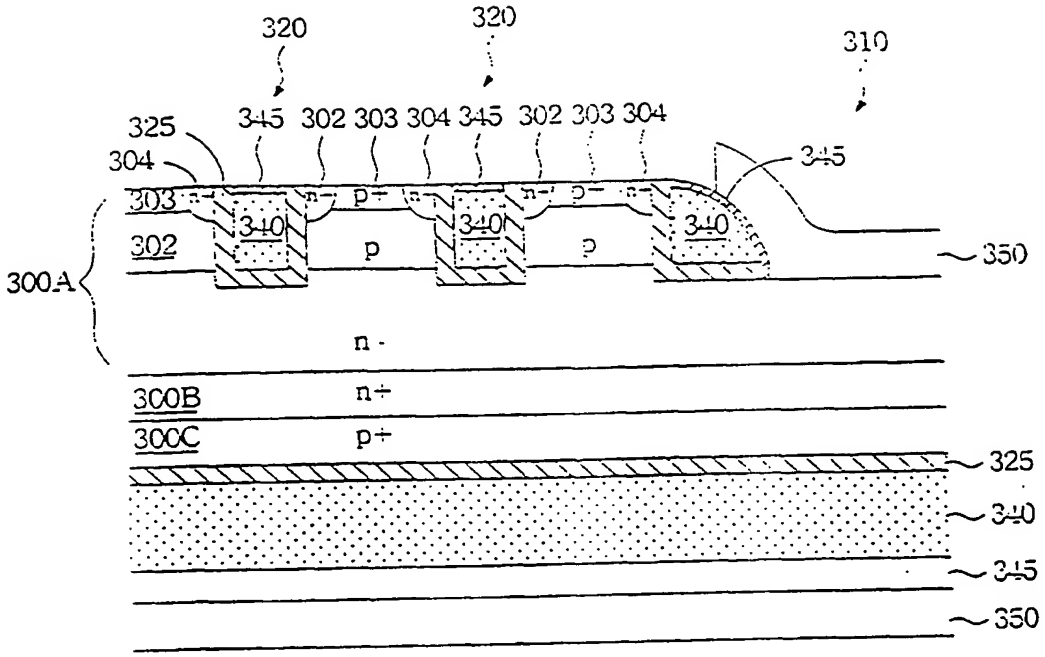
320
320
310
325
345
302
303
304
345
302
303
304
304
345
303
n+
p+
n+
n+
p+
n+
340
340
340
302
p
p
300A
350
n -
300B
n+
300C
p+
325
340
345
350

FIG.11

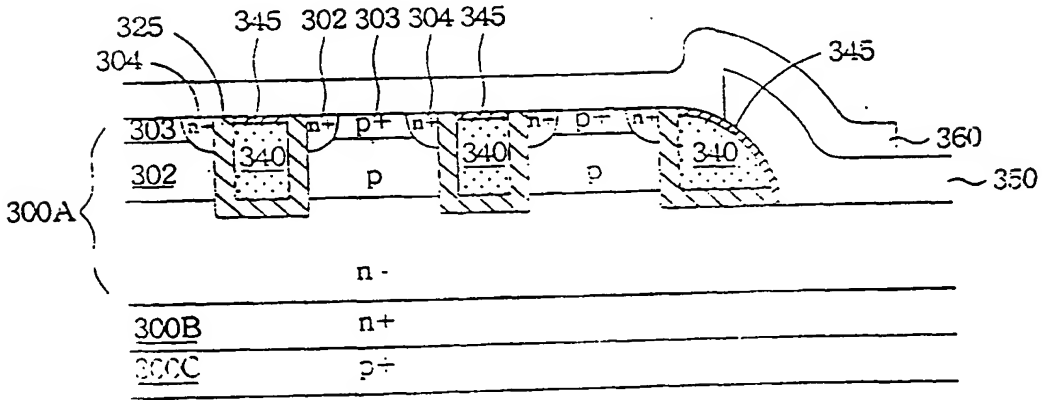
325
345
302
303
304
345
304
345
303
n+
n+
p+
n+
n+
p+
n+
340
340
340
360
302
p
p
350
300A
n -
300B
n+
300C
p+

FIG.12

(19) Europäisches Patentamt
European Patent Office
Office européen des brevets

(11) EP 1 191 603 A3

(12) EUROPEAN PATENT APPLICATION

(88) Date of publication A3:
17.11.2004 Bulletin 2004/47

(43) Date of publication A2:
27.03.2002 Bulletin 2002/13

(21) Application number: **01122746.9**

(22) Date of filing: **21.09.2001**

(51) Int Cl.[7]: **H01L 29/78**, H01L 29/739, H01L 29/872, H01L 29/06, H01L 21/336, H01L 21/331

(84) Designated Contracting States:
AT BE CH CY DE DK ES FI FR GB GR IE IT LI LU MC NL PT SE TR
Designated Extension States:
AL LT LV MK RO SI

(30) Priority: **22.09.2000 US 668663**

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(54) Trench MOS device and termination structure

(57) A termination structure for power trench MOS devices is disclosed. The MOS devices can be Schottky diode, IGBT or DMOS depending on what kinds of the semiconductor substrate are prepared. The termination structure comprises: a semiconductor substrate having a trench formed therein; a MOS gate as a spacer formed on a sidewall of the trench; a termination structure oxide layer formed in the trench to cover a portion of the spacer and to cover a bottom of the trench; and a first electrode and a second electrode are, respectively, formed on a bottom surface and upper surface of the semiconductor substrate. The trench is formed from a boundary of the active region to an end of the semiconductor substrate. The trench MOS devices are formed in the active region. In addition for IGBT and DMOS, the second electrode is isolated from MOS gate by an oxide layer; however, for Schottky diode, the second electrode is directed contact to the MOS gate.

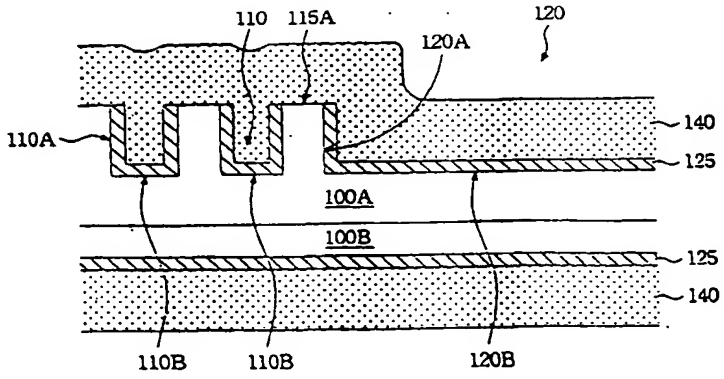

FIG.3

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EUROPEAN SEARCH REPORT

Application Number
EP 01 12 2746

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Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int.Cl.7)
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X	PATENT ABSTRACTS OF JAPAN vol. 1999, no. 08, 30 June 1999 (1999-06-30) -& JP 11 074524 A (DENSO CORP), 16 March 1999 (1999-03-16) * abstract; figure 8 * ---	1-6,8, 10-13, 15-17, 19,21,22	
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The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
MUNICH	20 September 2004	Lantier, R

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